REMARKS

Reconsideration of the application is requested.

Claims 1-8, 11-14 and 17 remain in the application. Claims 1-8, 11-14 and 17 are subject to examination. Claims 1 and 17 have been amended. Claims 9, 10, 15 and 16 have been canceled to facilitate prosecution of the instant application.

Under the heading "Claim Rejections - 35 USC § 102" on pages 2-3 of the above-identified Office Action, claims 1, 9, 10 and 17 have been rejected as being fully anticipated by U.S. Patent No. 5,953,641 to Auvray (hereinafter Auvray) under 35 U.S.C. § 102.

Independent claims 1 and 17 have been amended with the subject matter of original claims 9 and 10. Original claim 9 recites a reference frequency source commonly connected to the first and the second frequency generators. Original claim 10 recites that the first and second frequency generators are each a phase-locked loop having a local oscillator frequency set independently by a divider ratio.

According to the subject-matter of amended claims 1 and 17, a transmitting and receiving unit is provided. The transmitting and receiving unit contains a first frequency generator and a second frequency generator. A receiving branch has an in-

phase component and a quadrature component. The receiving branch has a first frequency converter coupled to the first frequency generator. A transmitting branch is also provided in the transmitting and receiving unit. The transmitting branch has an in-phase component and a quadrature component. The transmitting branch further includes a second frequency converter switchably coupled to one of the first and second frequency generators, respectively, through a switch. A control device is coupled to the switch for selecting a transmitting mode of operation and a receiving mode of operation.

Furthermore, according to the wording of amended claim 1, the first frequency generator includes a phase-locked loop. The phase-locked loop has a local oscillator frequency set by a divider ratio. The second frequency generator also contains a phase-locked loop having a local oscillator frequency. The local oscillator frequencies of the first and the second phase locked loops can be set independently by the respective divider ratios. As shown in Fig. 1 of the instant application, a first phase-locked loop 40 includes the oscillator 41, while the second phase-locked loop 30 has a different oscillator 31. Each PLL has measures 42,32 for providing divider ratios that can be set independently.

The transmitting and receiving unit further includes a

reference frequency source that is commonly connected to the first frequency generator and to the second frequency generator.

In full accordance with the Examiner's statement, Auvray does not contain two different phase-locked loops. Instead, only one single synthesizer SYN is provided in Fig. 1 of Auvray. Two different local oscillator frequencies are provided in Auvray using the single synthesizer. One frequency is provided by the synthesizer directly, while another frequency is provided using an additional divider DIV.

In conclusion, Auvray does not teach the feature of having two different phase-locked loops. Moreover, Auvray is silent on providing a common reference to different phase-locked loops.

According to the wording of amended claim 1 of the instant application, two different frequency generators include separate phase-locked loops. By doing this, different local oscillator frequencies can be provided at very high flexibility.

In addition to this, according to the wording of amended claim 1, the transceiver can be operated in two different modes. In one mode, both frequency converters in the receiving and transmitting branch are operated by the same local oscillator

frequency provided by one PLL. In another mode of operation, the frequency converter in the transceiving branch can be operated by a local oscillator frequency generated by a first PLL, while the converter in the receiving branch can be fed using a local oscillator frequency generated by a separate PLL in a different frequency converter.

The control device coupled to the switch is for selecting the respective mode of operation of the transceiver. By doing this, the above-mentioned flexibility of a frequency plan can be combined with very efficient power use.

Additional advantages are achieved using the above-described architecture in combination with a common reference frequency for the phase-locked loops. For example, the single PLL operation mode can be used if a direct conversion is applied both in transmit and receive path or if both transmit and receive path use a low-intermediate frequency (low-IF) structure. If for example the transmit branch operates in direct conversion (DC) mode and the receive branch in low IF mode, then two separate PLLs are activated. Also, for calibration of in-phase/quadrature (I/O) impairments, as described in the specification, two separate PLL frequency converters can be used.

In contrast, Auvray teaches only a single synthesizer. The

person of average skill in the art does not obtain any hint in Auvray to use different synthesizers with the switch architecture.

In conclusion, starting from Auvray, a person of average skill in the art cannot obtain a circuit having all features of the transceiver according to amended claim 1 of the instant application without performing an inventive step.

Please note that U.S. patent No. 6,795,690 82 to Weissman also contains a single local oscillator 40 permanently connected to converters both in the transmit and receive path.

U.S. patent No. 6,717,981 to Mohindra has only one local oscillator 120, but is silent on two different PLL circuits.

U.S. patent No. 5,862,181 to Ishizuka shows two different frequency generators 21, 25. However, these two frequency converters are permanently connected to the upconversion and downconversion means, respectively. Via an additional switch, a third frequency converter 23 can be fed with the sum or difference of the two local oscillator frequencies. Please also note that Ishizuka is silent in regards to a common reference frequency for the two oscillators 21, 25.

In conclusion, none of the prior art references teach the missing features of amended claim 1, namely to provide two frequency generators each having a phase-locked loop, and a switch to decide whether both transmitting and receiving frequency conversion is to be controlled via a single local oscillator frequency, or controlled using two different PLL circuits, depending on a desired mode. Moreover, none of the documents teaches to provide two PLL circuits with a common reference frequency.

Under the heading "Claim Rejections - 35 USC § 103" on pages 3-7 of the above-identified Office Action, claims 2-8 and 11-16 have been rejected as being obvious over at least one of U.S. Patent Nos. 5,953,641 to Auvray, 5,768,691 to Matero et al., 6,104,764 to Ohta et al., and 6,795,690 to Weissman et al. under 35 U.S.C. § 103.

As claims 2-8 and 11-16 ultimately depend on amended claim 1, claims 2-8 and 11-16 are believed to be allowable.

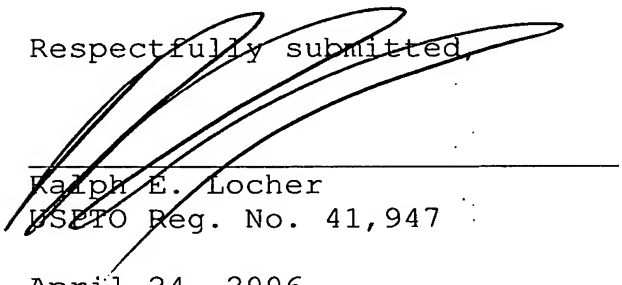
It is accordingly believed to be clear that none of the references, whether taken alone or in any combination, either show or suggest the features of claim 1 or 17. Claims 1 and 17 are, therefore, believed to be patentable over the art. The dependent claims are believed to be patentable as well because they all are ultimately dependent on claim 1.

In view of the foregoing, reconsideration and allowance of claims 1-8, 11-14 and 17 are solicited.

If an extension of time is required, petition for extension is herewith made. Any extension fee associated therewith should be charged to the Deposit Account of Lerner Greenberg Stemer, LLP, No. 12-1099.

Please charge any other fees that might be due with respect to Sections 1.16 and 1.17 to the Deposit Account of Lerner Greenberg Stemer, LLP, No. 12-1099.

Respectfully submitted,



Ralph E. Locher
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Lerner Greenberg Stemer, LLP
P.O. Box 2480
Hollywood, Florida 33022-2480
Tel.: (954) 925-1100
Fax: (954) 925-1101